REMARKS

Claims 1-33 are all the claims pending in the application.

I. Claim Rejections - 35 U.S.C. § 102

A. Rejections based on Sugita

The Examiner has rejected claims 1-12, 15-33 under 35 U.S.C. § 102(b) as being anticipated by Sugita (EP 744840 A2)) ["Sugita"]. For at least the following reasons, Applicant traverses the rejection.

Claim 1 requires that "reading the value of each bit stored in said storage means [be] at an arbitrary read timing ... based on discontinuous transmission within a code period."

The Examiner contends that Sugita performs the claimed "arbitrary timing of reading and writing to memory since the code or phrase varies" and cites col. 7, lines 6-19. Applicant submits that the cited section does not support an arbitrary timing for reading and writing as contended by the Examiner.

The cited section discloses the calculation of the state value of the long code PN code generator used for the next drive. Although the state value can vary, there is no disclosure or suggestion that the reading of this value from memory is done at an arbitrary timing. Sugita discloses that when timer 70 times out, the long code PN code generator 75 is operated from the state value which has been set (i.e. a read operation) (col. 9, lines 31-35). Therefore, at least the read operation is not arbitrary but based on timer 70.

Because independent claims 2, 11, 15, 16, 21 and 22 recite similar features as those given above, Applicant submits that these claims are patentable for at least reasons similar to those given above with respect to claim 1.

Applicant submits that claims 3-10, 12, 17-20 and 23-33 are patentable at least by virtue of their respective dependencies.

In addition claim 12 recites that the "first and second code generating circuits are the same circuit that is common to said transmission circuit and said reception circuit." The Examiner contends that section 3 and figs. 5, 7 and 8 disclose this feature, but does not provide any additional details. Applicant submits that these sections and figures do not disclose or suggest a system where the code generating circuits are the same circuit as set forth in claim 12.

With respect to claims 27-33, the Examiner contends that the reading and writing is arbitrary since the PN offset is arbitrary. Applicant submits that the cited sections do not support the position that any change in the offsets affects the startup of the code generator. Applicant submits that the startup of the code generator in Sugita is not arbitrary for at least reasons similar to those given above with respect to claim 1.

B. Rejections based on Easton

The Examiner has rejected claims 1-6, 11, 12, 15-33 under 35 U.S.C. § 102(e) as being anticipated by Easton et al. (US 6,590,886 B1) ["Easton"] (newly cited). For at least the following reasons, Applicant traverses the rejection.

Claim 1 requires that "reading the value of each bit stored in said storage means [be] at an arbitrary read timing ... based on discontinuous transmission within a code period." The

Examiner contends that the reading and writing is arbitrary since the values for determining the wake period is determined by the previous environment.

Easton discloses that the demodulator is enabled at 26.66 ms before the Slot boundary in order to initialize the decoder (read operation) (col. 6, lines 26-40). The Slot cycle, which determines the Slot boundary, is typically 1.28, 2.56 or 5.12 seconds in length (col. 4, lines 28-29). There is no disclosure or suggestion that the Slot cycle, once set, changes in the system. Therefore, Easton discloses that at least the reading of the PN code is not arbitrary but fixed at 26.66 ms before a Slot boundary based on the slot cycle of the system.

Because independent claims 2, 11, 15, 16, 21 and 22 recite similar features as those given above, Applicant submits that these claims are patentable for at least reasons similar to those given above with respect to claim 1.

Applicant submits that claims 3-6, 12, 17-20 and 23-33 are patentable at least by virtue of their respective dependencies.

In addition claim 12 recites that the "first and second code generating circuits are the same circuit that is common to said transmission circuit and said reception circuit." The Examiner contends that Easton discloses this feature, but does not provide any additional details. Applicant submits that Easton does not disclose or suggest a system where the code generating circuits are the same circuit as set forth in claim 12.

With respect to claims 27-33, the Examiner contends that the reading and writing is arbitrary since the startup time is different because the offset may change when the mobile wakes up. Applicant submits that the cited sections do not support the position that any change in the

offsets affects the startup of the code generator. Applicant submits that the startup of the code generator in Easton is not arbitrary for at least the reasons stated above with respect to claim 1.

II. Allowable Subject Matter

Applicant thanks the Examiner for allowing claim 14 and for finding allowable subject matter in claim 13. Claim 13 has been rewritten in independent form. Applicant submits that claim 13 is allowable.

III. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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